PD - 95813

International
IOR Rectifier

RADIATION HARDENED LOGIC LEVEL POWER MOSFET SURFACE MOUNT (UB)

IRHLUB770Z4 60V, N-CHANNEL

R7™ TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHLUB770Z4	100K Rads (Si)	0.55Ω	0.8A
IRHLUB730Z4	300K Rads (Si)	0.55Ω	0.8A
IRHLUB740Z4	600K Rads (Si)	0.55Ω	0.8A
IRHLUB780Z4	1000K Rads (Si)	0.55Ω	0.8A

UB

International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight
- Complimentary P-Channel Available - IRHLUB7970Z4

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 4.5V, T_C = 25°C	Continuous Drain Current	0.8	A
I_D @ V_{GS} = 4.5V, T_C = 100°C	Continuous Drain Current	0.5	
I_{DM}	Pulsed Drain Current ①	3.2	
P_D @ T_C = 25°C	Max. Power Dissipation	0.6	W
	Linear Derating Factor	0.0045	W/°C
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	2.0	mJ
I_{AR}	Avalanche Current ①	0.8	A
E_{AR}	Repetitive Avalanche Energy ①	0.06	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J	Operating Junction	-55 to 150	°C
T_{STG}	Storage Temperature Range		
	Lead Temperature	300 (for 5s)	
	Weight	43 (Typical)	mg

For footnotes refer to the last page

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.07	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.55	Ω	V_{GS} = 4.5V, I_D = 0.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	0.23	—	—	S (℧)	V_{DS} = 10V, I_{DS} = 0.5A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V_{DS}= 48V ,V_{GS}= 0V
		—	—	10		V_{DS} = 48V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -10V
Q_g	Total Gate Charge	—	—	3.6	nC	V_{GS} = 4.5V, I_D = 0.8A
Q_{gs}	Gate-to-Source Charge	—	—	1.5		V_{DS} = 30V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
$t_{d(on)}$	Turn-On Delay Time	—	—	8.0	ns	V_{DD} = 30V, I_D = 0.8A, V_{GS} = 4.5V, R_G = 24Ω
t_r	Rise Time	—	—	10		
$t_{d(off)}$	Turn-Off Delay Time	—	—	26		
t_f	Fall Time	—	—	10		
$L_S + L_D$	Total Inductance	—	8.4	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	166	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	42	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	3.5	—		
R_g	Gate Resistance	—	12	—	Ω	f = 5.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.8	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	3.2		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_j = 25°C, I_S = 0.8A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	70	ns	T_j = 25°C, I_F = 0.8A, di/dt ≤ 100A/μs
Q_{RR}	Reverse Recovery Charge	—	—	75	nC	V_{DD} ≤ 25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJA}	Junction-to-Case	—	—	220	°C/W	

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 600K Rads(Si)[1]		1000K Rads(Si)[2]		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	60	—	V	V_{GS} = 0V, I_D = 250µA
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0	1.0	2.0		V_{GS} = V_{DS}, I_D = 250µA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V_{GS} = 10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V_{GS} = -10 V
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	—	10	µA	V_{DS}= 48V, V_{GS} =0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.55	—	0.55	Ω	V_{GS} = 4.5V, I_D = 0.5A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (UB)	—	0.55	—	0.55	Ω	V_{GS} = 4.5V, I_D = 0.5A
V_{SD}	Diode Forward Voltage ④	—	1.2	—	1.2	V	V_{GS} = 0V, I_S = 0.8A

1. Part numbers IRHLUB770Z4, IRHLUB730Z4, IRHLUB740Z4
2. Part number IRHLUB780Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm2))	Energy (MeV)	Range (µm)	VDS (V) @VGS= 0V	@VGS= -2V	@VGS= -4V	@VGS= -5V	@VGS= -6V	@VGS= -7V	@VGS= -8V	@VGS= -10V
Br	37.3	285	36.8	60	60	60	60	60	35	30	20
I	59.9	345	32.7	60	60	60	60	60	20	15	-
Au	82.3	357	28.5	60	60	60	60	-	-	-	-

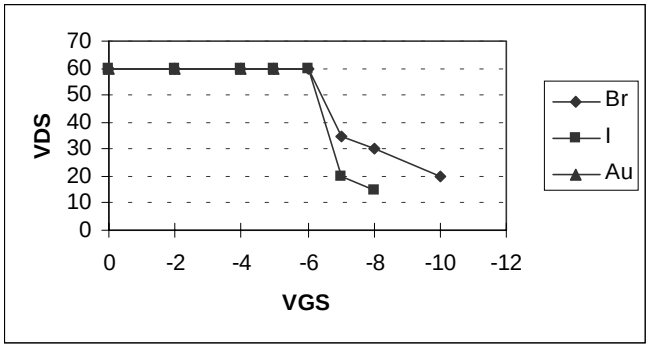


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

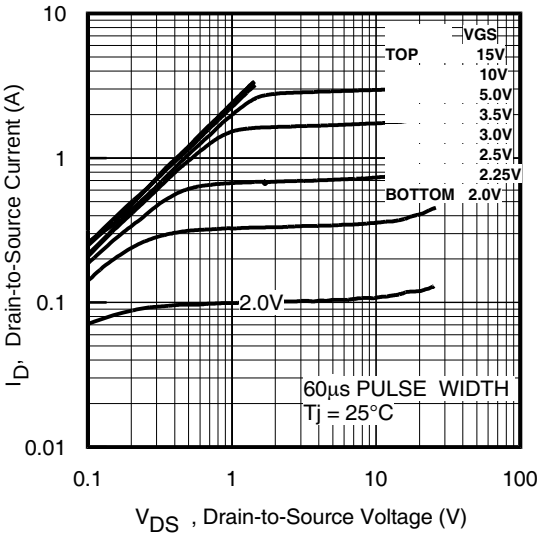


Fig 1. Typical Output Characteristics

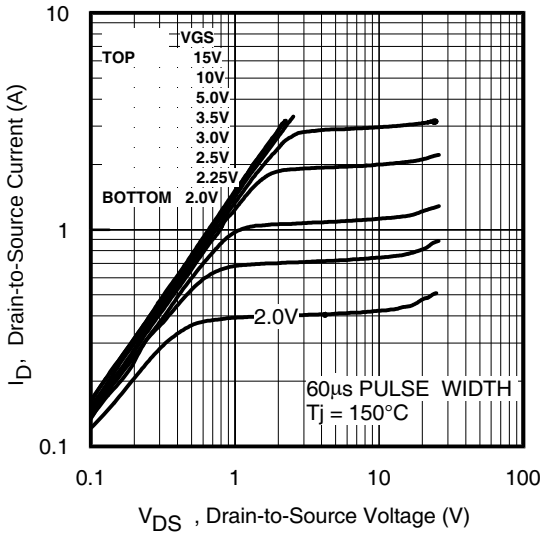


Fig 2. Typical Output Characteristics

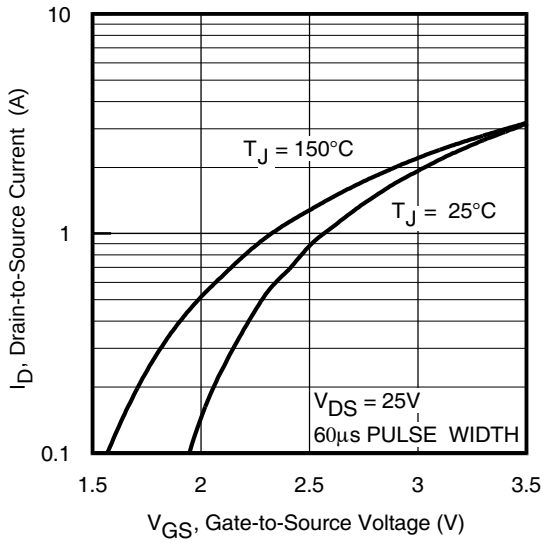


Fig 3. Typical Transfer Characteristics

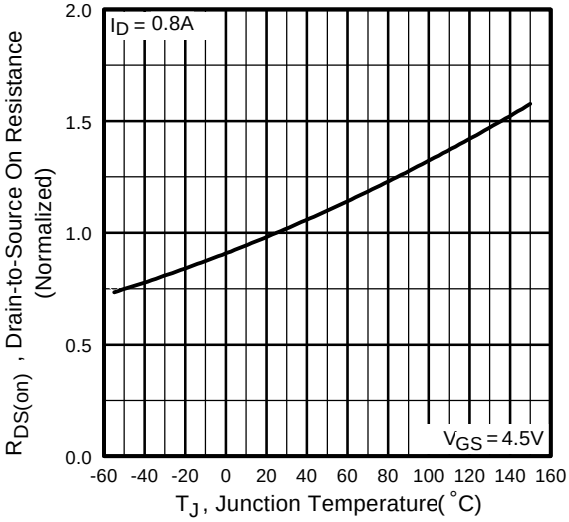


Fig 4. Normalized On-Resistance Vs. Temperature

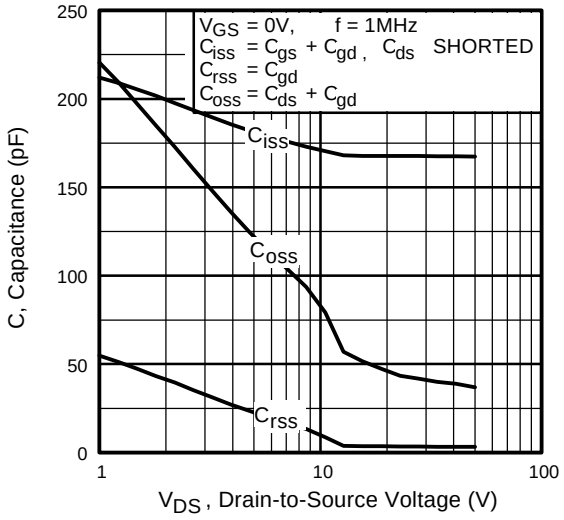


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

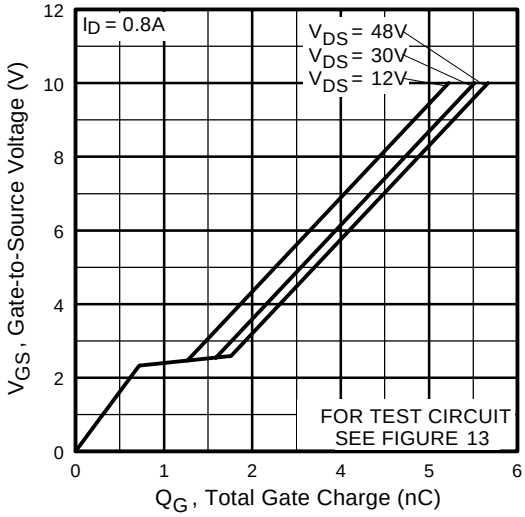


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

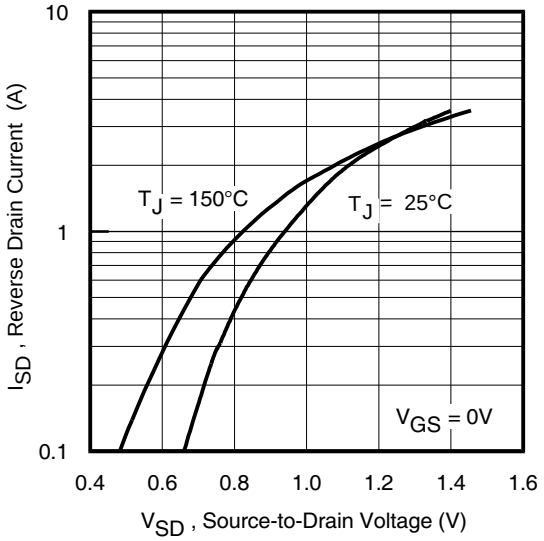


Fig 7. Typical Source-Drain Diode Forward Voltage

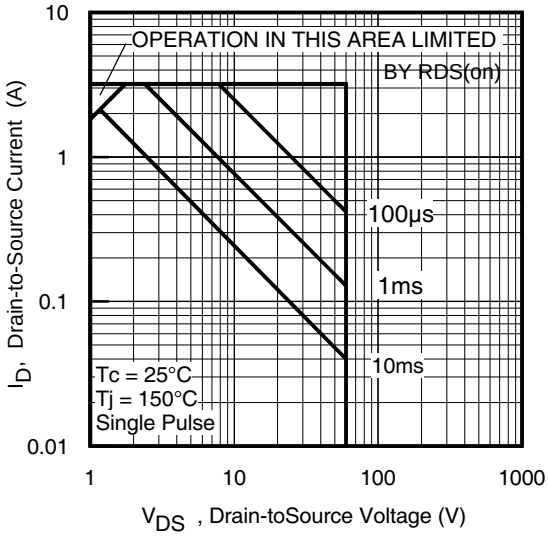


Fig 8. Maximum Safe Operating Area

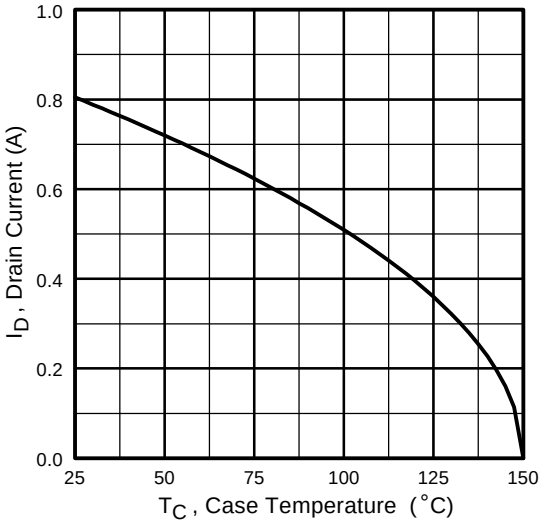


Fig 9. Maximum Drain Current Vs. Case Temperature

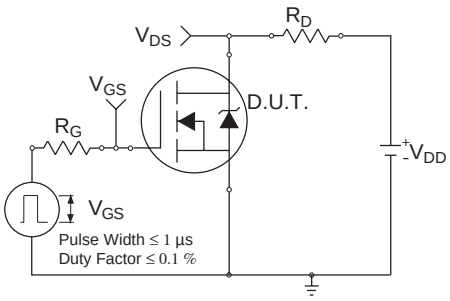


Fig 10a. Switching Time Test Circuit

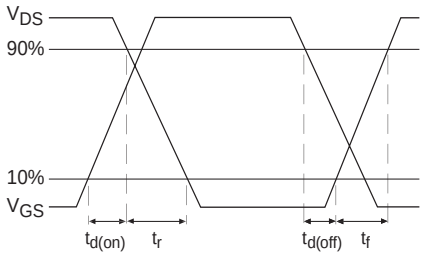


Fig 10b. Switching Time Waveforms

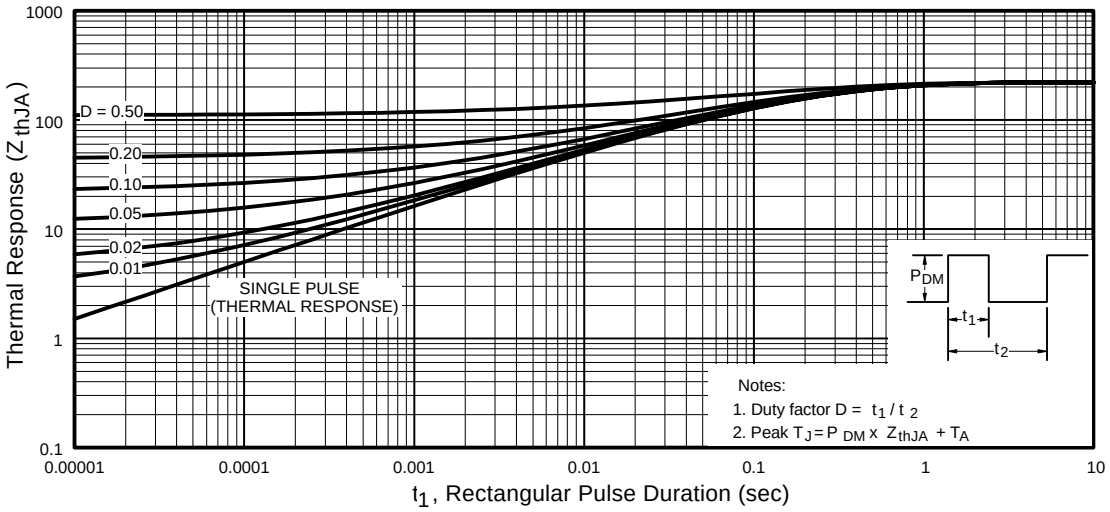


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

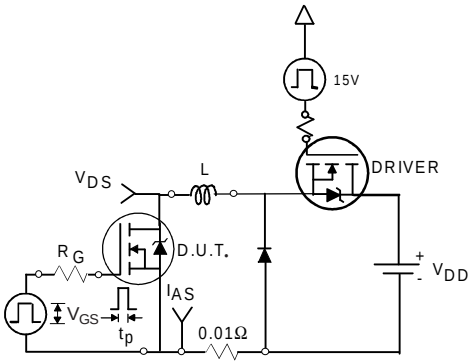


Fig 12a. Unclamped Inductive Test Circuit

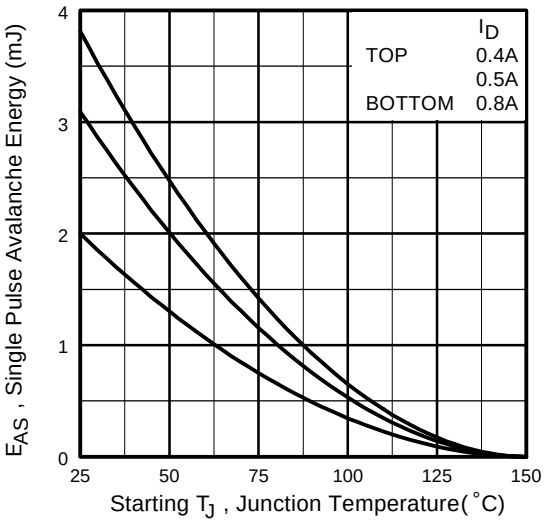


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

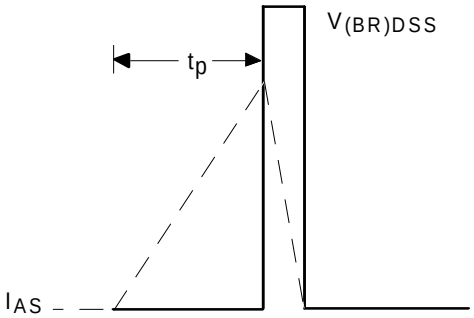


Fig 12b. Unclamped Inductive Waveforms

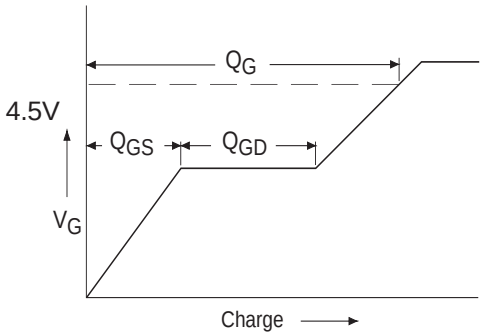


Fig 13a. Basic Gate Charge Waveform

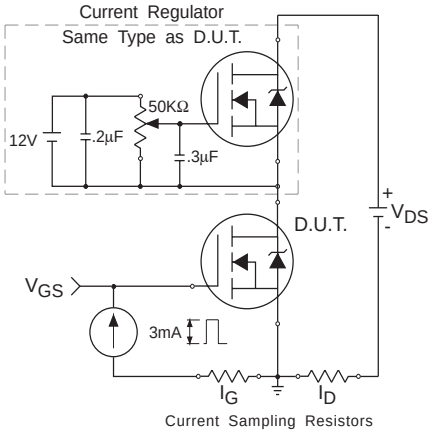


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L= 6.3 mH Peak I_L = 0.8A, V_{GS} = 10V

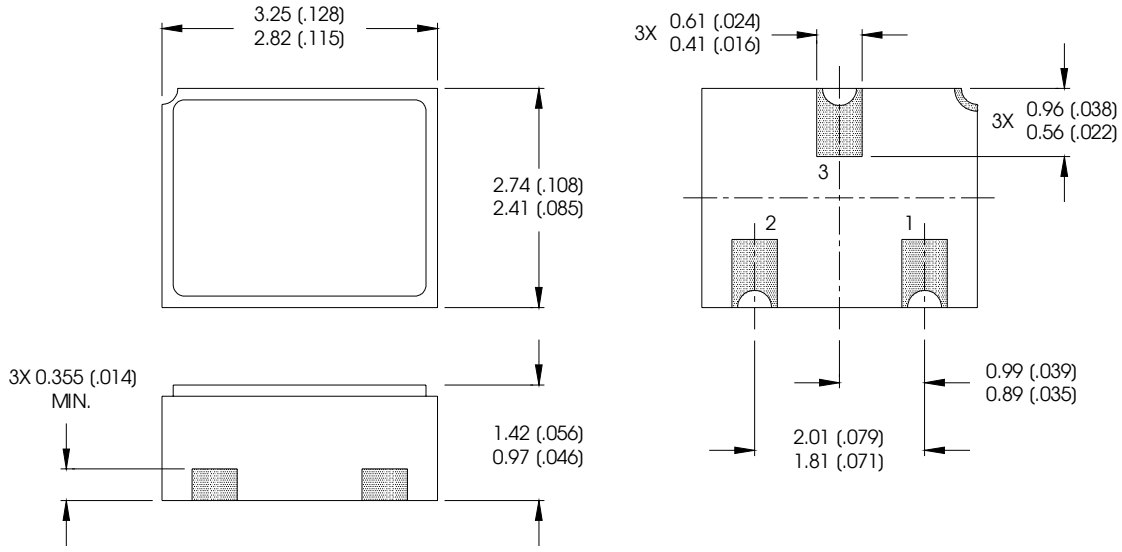
③ I_{SD} ≤ 0.8A, di/dt ≤ 130A/μs, V_{DD} ≤ 60V, T_J ≤ 150°C

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** 48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — UB



NOTES:

1. OUTLINE CONFORMS TO MIL-PRF-19500/255L
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. CONTROLLING DIMENSION: INCH.

PAD ASSIGNMENTS

1 = GATE
2 = SOURCE
3 = DRAIN

International
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